REMARKS

Claims 1-29 are currently pending in the subject application, and are presently under consideration. Claims 1-29 stand rejected. Favorable reconsideration of the application is requested in view of the comments herein.

I. Rejection of Claims 1-29 Under 35 U.S.C. §102(b)

Claims 1-29 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,345,379 to Khouja, et al. ("Khouja"). Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claim 1 recites area data associated with transistor gate area of at least one unit of a circuit design, and a power estimation engine that determines a relative estimation of power for the at least one unit of the circuit design based on a predetermined correlation that characterizes device power as a function of transistor gate area. The Office Action dated November 30, 2005, asserts that Khouja anticipates claim 1 (Office Action dated November 30, 2005, page 2). Representative for Applicant respectfully disagrees. Specifically, Khouja does not teach area data associated with transistor gate area of at least one unit of a circuit design, and a power estimation engine that determines a relative estimation of power for the at least one unit of the circuit design based on a predetermined correlation that characterizes device power as a function of transistor gate area.

As recited in claim 1, the term "transistor gate area" refers specifically to a physical area associated with the gate terminal of the transistor. This is evident in the Detailed Description of the Present Application: "the transistor gate area of a transistor can be computed by multiplying the width (W) by the length (L) of the transistor gate." (Present Application, page 4, ll. 18-19). Khouja teaches a method of quickly calculating power dissipation by a digital circuit using information available at a gate library level (Khouja, Abstract). The invention of Khouja, however, concerns itself with calculations of power dissipation on the cell level, and not the transistor level. Specifically, Khouja teaches as follows:

> The basic functional element of a digital design is a transistor. As digital design has progressed, the level of abstraction has been raised to the gate- or cell-level. A cell contains a collection of transistors connected into an electrical circuit that performs a combinational or sequential function. A typical cell might implement a NAND function or act as a D flip-flop. A design consists of an interconnected collection of cells. (Khouja, col. 4, ll. 26-33).

Accordingly, the term "gate" as used in the teachings of Khouja refers specifically to logic gates, and not a gate terminal associated with a transistor. This is further evident in the description of FIG. 12 of Khouja: "The circuit has multiple primary inputs I1-I9 and has multiple primary outputs $P0_0$, $P0_1$ and, $P0_2$ and has multiple gates N1-N10. Each gate is represented by a netlist node stored in memory." (Khouja, FIG. 12, col. 23, ll. 5-10). The "gates" described in this cited section refer specifically to logic gates, such as AND-gates and OR-gates, and not to gate terminals of transistors. Furthermore, Khouja teaches that "library developers can annotate gates with the approximate total leakage power that is dissipated by the gate, and that "[l]eakage power will be specified by a single cell-level attribute in the library..." (Khouja, col. 10, ll. 24-32). Power estimation, as taught by Khouja, is therefore applicable to estimation and calculation of power at the gate or cell level. Accordingly, the teachings of Khouja are unconcerned with a determination of power at the transistor level, and thus Khouja does not teach area data associated with transistor gate area of at least one unit of a circuit design and a predetermined correlation that characterizes device power as a function of transistor gate area, as recited in claim 1.

In addition, Khouja does not teach power estimation and/or calculation based on area data. Khouja teaches that a semiconductor vendor characterizes the electrical behavior of cells by providing estimates of delay through a cell and how much substrate area the cells will occupy, such that a library of components can be established for a designer to build a complex chip (Khouja, col. 2, ll. 7-12, col. 12, ll. 55-62). Khouja thus teaches that area data is merely used by circuit designers for laying out a complex circuit on a substrate, and not for power estimation and/or calculation. Therefore, Khouja does not teach area data associated with transistor gate area of at least one unit of a circuit design, and a power estimation engine that determines a

relative estimation of power for the at least one unit of the circuit design based on a predetermined correlation that characterizes device power as a function of transistor gate area, as recited in claim 1. Accordingly, Khouja does not anticipate claim 1. Withdrawal of the rejection of claim 1, as well as claims 2-12 which depend therefrom, is respectfully requested.

Claim 2 depends from claim 1, and further recites that the power estimation engine determines the relative estimation of power by employing at least one coefficient that characterizes device power as a function of transistor gate area. Khouja teaches coefficients associated with toggle rates and switching correlations (see Khouja, col. 20, line 43 through col. 21, line 7 and col. 39, ll. 1-4). However, Khouja does not teach at least one coefficient that characterizes device power as a function of transistor gate area, as recited in claim 2. Accordingly, Khouja does not anticipate claim 2.

Claim 3 depends from claim 2 and claim 1, and further recites that the at least one coefficient defines a substantially linear relationship between device power and transistor gate area, such that the at least one coefficient includes a multiplier coefficient and an offset coefficient. As described above, Khouja teaches coefficients associated with toggle rates and switching correlations, and does not teach at least one coefficient that characterizes device power as a function of transistor gate area. Assuming *arguendo* that the toggle rate and switching correlation coefficients can be construed as a characterization of device power as a function of transistor gate area, Khouja is silent as to estimation of device power through the use of a multiplier coefficient and an offset coefficient, such that a linear relationship is defined between device power and transistor gate area, as recited in claim 3. Accordingly, Khouja does not anticipate claim 3.

Claim 5 depends from claim 4 and claim 1, and further recites that the relative estimation of power is also based on a determination of gate leakage power. As described above with regard to claim 1, the teachings of Khouja are unconcerned with determining power consumption at the transistor level. Gate leakage current, as it is used in claim 5, refers to the "gate-to-source leakage current caused by tunneling effects into the gate oxide material of the gate, which increases as the gate oxide thickness decreases." (Present Application, page 1, ll. 31-33). Khouja

teaches a determination of leakage power for a cell, and not for individual transistors (see Khouja, col. 5, ll. 10-25). Therefore, Khouja does not teach that the relative estimation of power is also based on a determination of gate leakage power, as recited in claim 5. Accordingly, Khouja does not anticipate claim 5.

Claim 6 depends from claim 1, and further recites that area data includes high voltage threshold (HVT) transistor gate area data and low voltage threshold (LVT) transistor gate area data. A LVT transistor device is "used in performance-critical blocks to meet target clock frequency requirements." (Present Application, page 4, ll. 23-25). A HVT transistor device is used in blocks with delay slacks to minimize overall leakage power, such that HVT transistor devices have higher performance than LVT transistor devices (Present Application, page 4, ll. 25-28). Khouja teaches that a given input of a cell can be "in one of four states: held at a high voltage, held at a low voltage, transitioning from a high voltage to a low voltage, and transitioning from a low voltage to a high voltage." (Khouja, col. 4, ll. 55-58). However, Khouja is silent as to estimation of power of HVT and LVT transistor devices, and thus does not teach that area data includes HVT transistor gate area data and LVT transistor gate area data, as recited in claim 6. Accordingly, Khouja does not anticipate claim 6.

Claim 13 recites a first power estimator that determines an estimation of relative power associated with HVT devices by employing an HVT transistor gate area calculation and a predetermined functional relationship of HVT transistor gate area to HVT device power, and a second power estimator that determines an estimation of relative power associated with LVT devices by employing an LVT transistor gate area calculation and a predetermined functional relationship of LVT transistor gate area to LVT device power. As described above, Khouja is silent as to the estimation of power of HVT and LVT transistor devices. Also as described above, Khouja teaches that power estimation is applicable to estimation and calculation of power at the gate or cell level, and thus the teachings of Khouja are unconcerned with a determination of power at the transistor level. In addition, Khouja teaches that area data is merely used by circuit designers for laying out a complex circuit on a substrate, and not for power estimation and/or calculation. Therefore, Khouja does not teach estimation of relative power associated

with HVT devices by employing an HVT transistor gate area calculation and a predetermined functional relationship of HVT transistor gate area to HVT device power, and a second power estimator that determines an estimation of relative power associated with LVT devices by employing an LVT transistor gate area calculation and a predetermined functional relationship of LVT transistor gate area to LVT device power, as recited in claim 13. Accordingly, Khouja does not anticipate claim 13. Withdrawal of the rejection of claim 13, as well as claims 14-18 which depend therefrom, is respectfully requested.

Claim 14 depends from claim 13, and further recites a third power estimator that determines an estimation of relative power associated with LVT and HVT device gate leakage by employing the LVT transistor gate area calculation and the HVT transistor gate area calculation and a predetermined functional relationship of LVT and HVT transistor gate area to gate leakage power. As described above, Khouja teaches a determination of leakage power for a cell, and not for gate-to-source leakage of individual transistors. Therefore, Khouja does not teach a third power estimator that determines an estimation of relative power associated with LVT and HVT device gate leakage by employing the LVT transistor gate area calculation and the HVT transistor gate area calculation and a predetermined functional relationship of LVT and HVT transistor gate area to gate leakage power, as recited in claim 14. Accordingly, Khouja does not anticipate claim 14.

Claim 16 depends from claim 14 and claim 13, and further recites that the first power estimator and the second power estimator employ dynamic and static weight factors in determining the weight associated with the static and dynamic power estimates. Khouja teaches that switching power of a given cell can be calculated by determining a transition time using weighted toggle rates (Khouja, col. 11, ll. 8-18). However, Khouja does not teach that the first power estimator and the second power estimator employ dynamic and static weight factors in determining the weight associated with the static and dynamic power estimates, as recited in claim 16. Accordingly, Khouja does not anticipate claim 16.

Claim 19 recites means for characterizing power as a function of circuit transistor gate area, means for generating transistor gate area calculations for a plurality of circuit sizing

instances associated with a circuit design, and means for computing relative power estimates of the plurality of circuit sizing instances employing the transistor gate area calculations and the characterization of power as a function of circuit transistor gate area. As described above, Khouja teaches that power estimation is applicable to estimation and calculation of power at the gate or cell level, and thus the teachings of Khouja are unconcerned with a determination of power at the transistor level. In addition, Khouja teaches that area data is merely used by circuit designers for laying out a complex circuit on a substrate, and not for power estimation and/or calculation. Therefore, Khouja does not teach means for characterizing power as a function of circuit transistor gate area, means for generating transistor gate area calculations for a plurality of circuit sizing instances associated with a circuit design, and means for computing relative power estimates of the plurality of circuit sizing instances employing the transistor gate area calculations and the characterization of power as a function of circuit transistor gate area, as recited in claim 19. Accordingly, Khouja does not anticipate claim 19. Withdrawal of the rejection of claim 19, as well as claims 20-22, which depend therefrom, is respectfully requested.

Claim 20 depends from claim 19, and further recites that the means for characterizing power as a function of circuit transistor gate area comprising a first characterizing of power as a function of HVT transistor gate area, a second characterizing of power as a function of LVT transistor gate area, and a third characterization of gate device leakage power based on LVT transistor gate area and HVT transistor gate area. As described above, Khouja is silent as to the estimation of power of HVT and LVT transistor devices. Also as described above, Khouja teaches a determination of leakage power for a cell, and not for gate-to-source leakage of individual transistors. Therefore, Khouja does not teach means for characterizing power as a function of circuit transistor gate area comprising a first characterizing of power as a function of HVT transistor gate area, a second characterizing of power as a function of LVT transistor gate area, and a third characterization of gate device leakage power based on LVT transistor gate area and HVT transistor gate area, as recite in claim 20. Accordingly, Khouja does not anticipate claim 20.

Claim 23 recites calculating the transistor gate area associated with a circuit design, and estimating relative power by computing a predetermined characterization of power as a function of transistor gate area. As described above, Khouja teaches that power estimation is applicable to estimation and calculation of power at the gate or cell level, and thus the teachings of Khouja are unconcerned with a determination of power at the transistor level. In addition, Khouja teaches that area data is merely used by circuit designers for laying out a complex circuit on a substrate, and not for power estimation and/or calculation. Therefore, Khouja does not teach calculating the transistor gate area associated with a circuit design, and estimating relative power by computing a predetermined characterization of power as a function of transistor gate area, as recited in claim 23. Accordingly, Khouja does not anticipate claim 23. Withdrawal of the rejection of claim 23, as well as claims 24-29, which depend therefrom, is respectfully requested.

Claim 24 depends from claim 23, and further recites that the predetermined characterization of power as a function of transistor gate area being a substantially linear relationship that employs at least one of a multiplier coefficient and an offset coefficient to define power as a function of transistor gate area. As described above, Khouja teaches coefficients associated with toggle rates and switching correlations, and does not teach estimation of device power through the use of a multiplier coefficient and an offset coefficient. Therefore, Khouja does not teach that the predetermined characterization of power as a function of transistor gate area being a substantially linear relationship that employs at least one of a multiplier coefficient and an offset coefficient to define power as a function of transistor gate area, as recited in claim 24. Accordingly, Khouja does not anticipate claim 24.

Claim 25 depends from claim 23, and further recites that the estimating relative power by computing a predetermined characterization of power as a function of transistor gate area comprising computing a first predetermined function of power based on HVT transistor gate area for HVT devices and by computing a second predetermined function of power based on LVT transistor gate area for LVT. As described above, Khouja is silent as to the estimation of power of HVT and LVT transistor devices. Therefore, Khouja does not teach that the estimating relative power by computing a predetermined characterization of power as a function of

transistor gate area comprising computing a first predetermined function of power based on HVT transistor gate area for HVT devices and by computing a second predetermined function of power based on LVT transistor gate area for LVT, as recited in claim 25. Accordingly, Khouja does not anticipate claim 25.

Claim 26 depends from claim 25 and claim 23, and further recites that the estimating relative power by computing a predetermined characterization of power as a function of transistor gate area comprises estimating power by computing a third predetermined function of gate leakage power based on transistor gate area for both HVT devices and LVT devices. As described above, Khouja teaches a determination of leakage power for a cell, and not for gate-to-source leakage of individual transistors. Therefore, Khouja does not teach that the estimating relative power by computing a predetermined characterization of power as a function of transistor gate area comprises estimating power by computing a third predetermined function of gate leakage power based on transistor gate area for both HVT devices and LVT devices, as recited in claim 26. Accordingly, Khouja does not anticipate claim 26.

Claim 27 depends from claim 25 and claim 23, and further recites that the first predetermined function of power and the second predetermined function of power compute both static and dynamic power based on weights associated with both static and dynamic power. As described above, Khouja teaches that switching power of a given cell can be calculated by determining a transition time using weighted toggle rates, but does not teach estimating power by employing dynamic and static weight factors in determining the weight associated with the static and dynamic power estimates. Therefore, Khouja does not teach that the first predetermined function of power and the second predetermined function of power compute both static and dynamic power based on weights associated with both static and dynamic power, as recited in claim 27. Accordingly, Khouja does not anticipate claim 27.

For the reasons described above, claims 1-29 should be patentable over the cited art. Accordingly, withdrawal of this rejection is respectfully requested.

CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that the present application is in condition for allowance. Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

Should the Examiner have any questions concerning this paper, the Examiner is invited and encouraged to contact Applicant's undersigned attorney at (216) 621-2234, Ext. 106.

No additional fees should be due for this response. In the event any fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to Deposit Account No. 08-2025.

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